19-1053; Rev 1; 3/08

Single/Dual, 16ns, High Sink/Source Current Gate Drivers

General Description

The MAX15024/MAX15025 single/dual, high-speed MOSFET gate drivers are capable of operating at frequencies up to 1MHz with large capacitive loads. The MAX15024 includes internal source-and-sink output transistors with independent outputs allowing for control of the external MOSFET's rise and fall time. The MAX15024 is a single gate driver capable of sinking an 8A peak current and sourcing a 4A peak current. The MAX15025 is a dual gate driver capable of sinking a 4A peak current and sourcing a 2A peak current. An integrated adjustable LDO voltage regulator provides gate-drive amplitude control and optimization.

The MAX15024A/C and MAX15025A/C/E/G accept transistor-to-transistor (TTL) input logic levels while the MAX15024B/D and MAX15025B/D/F/H accept CMOS-input logic levels. High sourcing/sinking peak currents, a low propagation delay, and thermally enhanced packages make the MAX15024/MAX15025 ideal for high-frequency and high-power circuits. The MAX15024/MAX15025 operate from a 4.5V to 28V supply. A separate output driver supply input enhances flexibility and permits a soft-start of the power MOSFETs used in synchronous rectifiers.

The MAX15024/MAX15025 are available in 10-pin TDFN packages and are specified over the -40°C to +125°C automotive temperature range.

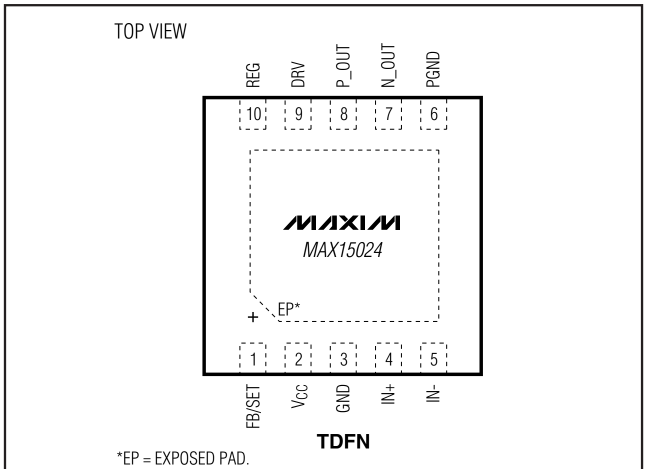
Applications

Synchronous Rectifier Drivers

Power-Supply Modules

Switching Power Supply

Pin Configurations



Pin Configurations continued at end of data sheet.

Features

- ♦ 8A Peak Sink Current/4A Peak Source Current (MAX15024)
- ♦ 4A Peak Sink Current/2A Peak Source Current (MAX15025)
- ♦ Low 16ns Propagation Delay
- ♦ 4.5V to 28V Supply Voltage Range
- ♦ On-Board Adjustable LDO for Gate-Drive Amplitude Control and Optimization
- ♦ Separate Output Driver Supply
- ♦ Independent Source and Sink Outputs (MAX15024)
- ♦ Matched Delays Between Inverting and Noninverting Inputs (MAX15024)
- ♦ Matched Delays Between Channels (MAX15025)
- ♦ CMOS or TTL Logic-Level Inputs with Hysteresis for Noise Immunity
- ♦ -40°C to +125°C Operating Temperature Range
- ♦ Thermal-Shutdown Protection
- ♦ 1.95W Thermally Enhanced TDFN Power Packages

Ordering Information

PART	PIN-PACKAGE	PKG CODE	TOP MARK
MAX15024AATB+T	10 TDFN-EP**	T1033-1	ATX
MAX15024BATB+T	10 TDFN-EP**	T1033-1	ATY
MAX15024CATB+T*	10 TDFN-EP**	T1033-1	—
MAX15024DATB+T*	10 TDFN-EP**	T1033-1	—
MAX15025AATB+T	10 TDFN-EP**	T1033-1	ATZ
MAX15025BATB+T	10 TDFN-EP**	T1033-1	AUA
MAX15025CATB+T	10 TDFN-EP**	T1033-1	AUB
MAX15025DATB+T	10 TDFN-EP**	T1033-1	AUC
MAX15025EATB+T*	10 TDFN-EP**	T1033-1	—
MAX15025FATB+T*	10 TDFN-EP**	T1033-1	—
MAX15025GATB+T*	10 TDFN-EP**	T1033-1	—
MAX15025HATB+T*	10 TDFN-EP**	T1033-1	—

Note: *All devices are specified over the -40°C to +125°C operating temperature range.*

+Denotes a lead-free package.

**Future product—contact factory for availability.*

***EP = Exposed pad. T = Tape and reel.*

See the Selector Guide at the end of the data sheet.

Block Diagrams appear at end of data sheet.

Single/Dual, 16ns, High Sink/Source Current Gate Drivers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ....-0.3V to +30V
REG to GND ....-0.3V to the lower of +22V or (V_{CC} + 0.3V)
DRV to PGND ....-0.3V to +22V
IN_ ....-0.3V to +22V
FB/SET to GND ....-0.3V to +6V
P_OUT to DRV ....-22V to +0.3V
N_OUT to PGND ....-0.3V to +22V
OUT1, OUT2 to PGND ....-0.3V to (V_{DRV} + 0.3V)
PGND to GND ....-0.3V to +0.3V
P_OUT, N_OUT Continuous Source/Sink Current* 200mA
OUT1, OUT2 Continuous Source/Sink Current* 200mA
Continuous Power Dissipation (T_A = +70°C)
10-Pin TDFN, Single-Layer Board
(derate 18.5mW/°C above +70°C) 1481.5mW
Junction-to-Case Thermal Resistance (Note 1) ....8.5°C/W
10-Pin TDFN, Multilayer Board
(derate 24.4mW/°C above +70°C) 1951.2mW
Junction-to-Case Thermal Resistance (Note 1) ....8.5°C/W
Operating Temperature Range ....-40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

**Continuous output current is limited by the power dissipation of the package.*

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, see **www.maxim-ic.com/thermal.tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAX15024 ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{DRV} = V_{REG} = 10V, FB/SET = GND, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = + 25°C). (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYSTEM SPECIFICATIONS							
Input Voltage Range	V_{CC}	V_{CC} powered only, V_{REG} = V_{DRV} decoupled with minimum 1µF to GND	MAX15024B/D	6.5		28.0	V
			MAX15024A/C	4.5		28.0	
		V_{CC} = V_{REG} = V_{DRV} (MAX15024D)		6.5		18.0	
		V_{CC} = V_{REG} = V_{DRV} (MAX15024C)		4.5		18.0	
V_{DRV} Turn-On Voltage	V_{DRV_ON}	V_{CC} = V_{REG} = 10V, IN+ = V_{CC}, IN- = GND			1.7	2.3	V
Quiescent Supply Current		IN_ = V_{CC} or GND			700	1350	µA
Quiescent Supply Current Under UVLO Condition		IN_ = V_{CC} or GND			250		µA
Switching Supply Current		Switching at 250kHz, C_L = 0			1.5	3.0	mA
V_{CC} Undervoltage Lockout	UVLO_ V_{CC}	V_{CC} rising		3.0	3.4	3.8	V
V_{CC} Undervoltage-Lockout Hysteresis					300		mV
V_{CC} Undervoltage Lockout to Output Delay		V_{CC} rising			100		µs
		V_{CC} falling			2		
REG REGULATOR (V_{CC} = 12V, REG = V_{DRV}, C_L = 1µF, FB/SET = GND)							
Output Voltage	V_{REG}	12V < V_{CC} < 28V, 0 < I_{LOAD} < 10mA		9	10	11	V
Dropout Voltage	V_{R_DO}	V_{CC} = 6.5V, I_{LOAD} = 100mA			0.4	0.9	V
		V_{CC} = 4.5V, I_{LOAD} = 50mA			0.2	0.5	
Load Regulation		V_{CC} = 12V, I_{LOAD} = 0 to 100mA			1		%
Line Regulation		12V < V_{CC} < 28V			10		mV
FB/SET Reference Voltage		External resistive divider connected at FB/SET		1.10	1.23	1.35	V
FB/SET Threshold		V_{FB} falling			220		mV
FB/SET Input Leakage Current		V_{FB} = 4.5V (Note 3)		-125		+125	nA

MAX15024 ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{DRV} = V_{REG} = 10V, FB/SET = GND, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = + 25°C). (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER OUTPUT (SINK)							
Driver Output Resistance	R_{ON-N}	V_{CC} = V_{REG} = V_{DRV} = 10V, sinking 100mA	T_A = +25°C		0.45	0.60	Ω
			T_A = +125°C		0.625	0.850	
		V_{CC} = V_{REG} = V_{DRV} = 4.5V, sinking 100mA (MAX15024C/D)	T_A = +25°C		0.50	0.65	
			T_A = +125°C		0.7	0.9	
Peak Output Current	I_{PK-N}	V_{N_OUT} = 10V			8		A
Maximum Load Capacitance		SOA condition: C_L x V_{DRV}^2 ≤ 20µJ, for V_{DRV} = 10V			200		nF
Latchup Robustness					500		mA
DRIVER OUTPUT (SOURCE)							
Driver Output Resistance	R_{ON-P}	V_{CC} = V_{REG} = V_{DRV} = 10V, sourcing 100mA	T_A = +25°C		0.875	1.500	Ω
			T_A = +125°C		1.2	2.0	
		V_{CC} = V_{REG} = V_{DRV} = 4.5V, sourcing 100mA (MAX15024C/D)	T_A = +25°C		0.95	1.65	
			T_A = +125°C		1.25	2.20	
Peak Output Current	I_{PK-P}	V_{P_OUT} = 0V			4		A
Latchup Robustness					500		mA
LOGIC INPUTS							
Logic 1 Input Voltage	V_{IH}	MAX15024A/C		2.0			V
		MAX15024B/D		4.25			
Logic 0 Input Voltage	V_{IL}	MAX15024A/C				0.8	V
		MAX15024B/D				2	
Logic Input Hysteresis		MAX15024A/C			0.4		V
		MAX15024B/D			1		
Logic Input Current Leakage		V_{IN} = 18V or GND		-75	0.01	+75	µA
Input Capacitance					10		pF
SWITCHING CHARACTERISTICS FOR V_{CC} = V_{DRV} = V_{REG} = 10V, P_OUT AND N_OUT ARE CONNECTED TOGETHER (see Figure 1)							
Rise Time	t_R	C_{LOAD} = 1nF			3		ns
		C_{LOAD} = 5nF			12		
		C_{LOAD} = 10nF			24		
Fall Time	t_F	C_{LOAD} = 1nF			3		ns
		C_{LOAD} = 5nF			8		
		C_{LOAD} = 10nF			16		
Turn-On Delay Time	t_{D-ON}	C_{LOAD} = 1nF (Note 3)		8	16	32	ns
Turn-Off Delay Time	t_{D-OFF}	C_{LOAD} = 1nF (Note 3)		8	16	32	ns
Mismatch Propagation Delays from Inverting and Noninverting Inputs to Output		C_{LOAD} = 1nF			1		ns

Single/Dual, 16ns, High Sink/Source Current Gate Drivers

MAX15024 ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{DRV} = V_{REG} = 10V, FB/SET = GND, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = + 25°C). (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS FOR V_{CC} = V_{DRV} = V_{REG} = 4.5V (see Figure 1) (MAX15024C/D)						
Rise Time	t_R	C_{LOAD} = 1nF		3		ns
		C_{LOAD} = 5nF		11		
		C_{LOAD} = 10nF		22		
Fall Time	t_F	C_{LOAD} = 1nF		2.5		ns
		C_{LOAD} = 5nF		8		
		C_{LOAD} = 10nF		16		
Turn-On Delay Time	t_{D-ON}	C_{LOAD} = 1nF		18		ns
Turn-Off Delay Time	t_{D-OFF}	C_{LOAD} = 1nF		18		ns
Mismatch Propagation Delays from Inverting and Noninverting Inputs to Output		C_{LOAD} = 1nF		2		ns
Minimum Input Pulse Width that Changes the Output	t_{PW}			15		ns
THERMAL CHARACTERISTICS						
Thermal-Shutdown Temperature		Temperature rising		+160		°C
Thermal-Shutdown Temperature Hysteresis				15		°C

MAX15025 ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{DRV} = V_{REG} = 10V, FB/SET = GND, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C). (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYSTEM SPECIFICATIONS							
Input Voltage Range	V_{CC}	V_{CC} powered only, V_{REG} = V_{DRV} decoupled with minimum 1µF to GND	MAX15025B/D/F/H		6.5	28	V
			MAX15025A/C/E/G		4.5	28	
		V_{CC} = V_{REG} = V_{DRV} (MAX15025F/H)		6.5		18.0	
		V_{CC} = V_{REG} = V_{DRV} (MAX15025E/G)		4.5		18.0	
V_{DRV} Turn-On Voltage	V_{DRV_ON}	V_{CC} = V_{REG} = 10V, IN1 = V_{CC}, IN2 = V_{CC} (MAX15025A/B/E/F) or GND for (MAX15025C/D/G/H)			1.7	2.3	V
Quiescent Supply Current		IN_ = V_{CC} or GND			700	1350	µA
Quiescent Supply Current Under UVLO Condition		IN_ = V_{CC} or GND			250		µA
Switching Supply Current		Switching at 250kHz, C_L = 0			1.5	3.0	mA
V_{CC} Undervoltage Lockout	UVLO_ V_{CC}	V_{CC} rising		3.0	3.4	3.8	V

MAX15025 ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{DRV} = V_{REG} = 10V, FB/SET = GND, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C). (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Undervoltage-Lockout Hysteresis					300		mV
V_{CC} Undervoltage Lockout to Output Delay		V_{CC} rising			100		µs
		V_{CC} falling			2		
REG REGULATOR (V_{CC} = 12V, V_{REG} = V_{DRV}, C_L = 1µF, FB/SET = GND)							
Output Voltage	V_{REG}	12V < V_{CC} < 28V, 0 < I_{LOAD} < 10mA		9	10	11	V
Dropout Voltage	V_{R_DO}	V_{CC} = 6.5V, I_{LOAD} = 100mA			0.4	0.9	V
		V_{CC} = 4.5V, I_{LOAD} = 50mA			0.2	0.5	
Load Regulation		V_{CC} = 12V, I_{LOAD} = 0 to 100mA			1		%
Line Regulation		12V < V_{CC} < 28V			10		mV
FB/SET Reference Voltage		External resistive divider connected at FB/SET		1.10	1.23	1.35	V
FB/SET Threshold		V_{FB} rising			220		mV
FB/SET Input Leakage Current		V_{FB} = 4.5V		-125		+125	nA
DRIVER OUTPUT SINK							
Driver Output Resistance	R_{ON-N}	V_{CC} = V_{REG} = V_{DRV} = 10V, sinking 100mA	T_A = +25°C		1.0	1.6	Ω
			T_A = +125°C		1.25	2.10	
		V_{CC} = V_{REG} = V_{DRV} = 4.5V, sinking 100mA (MAX15025E/F/G/H)	T_A = +25°C		1.10	1.65	
			T_A = +125°C		1.5	2.2	
Peak Output Current	I_{PK-N}	$V_{OUT\_}$ = 10V			4		A
Maximum Load Capacitance		SOA condition: $C_L \times V_{DRV}^2 \leq 20µJ$, for V_{DRV} = 10V			100		nF
Latchup Robustness					500		mA
DRIVER OUTPUT SOURCE							
Driver Output Resistance	R_{ON-P}	V_{CC} = V_{REG} = V_{DRV} = 10V, sourcing 100mA	T_A = +25°C		1.75	2.50	Ω
			T_A = +125°C		2.25	3.50	
		V_{CC} = V_{REG} = V_{DRV} = 4.5V, sourcing 100mA (MAX15025E/F/G/H)	T_A = +25°C		1.85	2.60	
			T_A = +125°C		2.50	3.75	
Peak Output Current	I_{PK-P}	$V_{OUT\_}$ = 0V			2		A
Latchup Robustness					500		mA
LOGIC INPUTS							
Logic 1 Input Voltage	V_{IH}	MAX15025A/C/E/G		2.0			V
		MAX15025B/D/F/H		4.25			
Logic 0 Input Voltage	V_{IL}	MAX15025A/C/E/G				0.8	V
		MAX15025B/D/F/H				2	
Logic Input Hysteresis		MAX15025A/C/E/G			0.4		V
		MAX15025B/D/F/H			1		
Logic Input Current Leakage		V_{IN} = 18V or GND		-75	+0.01	+75	µA
Input Capacitance					10		pF

MAX15025 ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{DRV} = V_{REG} = 10V, FB/SET = GND, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C). (Note 2)

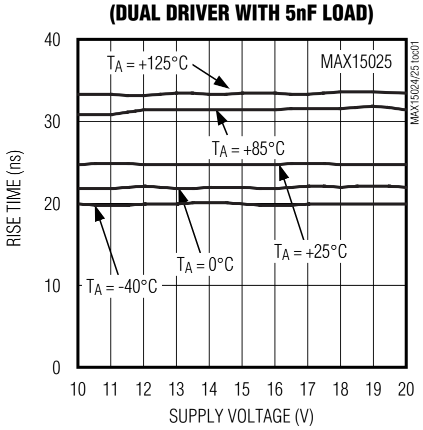
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS FOR V_{CC} = V_{DRV} = V_{REG} = 10V (see Figure 1)						
Rise Time	t_R	C_{LOAD} = 1nF		6		ns
		C_{LOAD} = 5nF		24		
		C_{LOAD} = 10nF		48		
Fall Time	t_F	C_{LOAD} = 1nF		5		ns
		C_{LOAD} = 5nF		16		
		C_{LOAD} = 10nF		32		
Turn-On Delay Time	t_{D-ON}	C_{LOAD} = 1nF (Note 3)	8	16	32	ns
Turn-Off Delay Time	t_{D-OFF}	C_{LOAD} = 1nF (Note 3)	8	16	32	ns
Mismatch Propagation Delays Between 2 Channels		C_{LOAD} = 1nF		1		ns
SWITCHING CHARACTERISTICS FOR V_{CC} = V_{DRV} = V_{REG} = 4.5V (see Figure 1) (MAX15025E/F/G/H)						
Rise Time	t_R	C_{LOAD} = 1nF		5		ns
		C_{LOAD} = 5nF		20		
		C_{LOAD} = 10nF		42		
Fall Time	t_F	C_{LOAD} = 1nF		4		ns
		C_{LOAD} = 5nF		15		
		C_{LOAD} = 10nF		30		
Turn-On Delay Time	t_{D-ON}	C_{LOAD} = 1nF		18		ns
Turn-Off Delay Time	t_{D-OFF}	C_{LOAD} = 1nF		18		ns
Mismatch Propagation Delays Between 2 Channels		C_{LOAD} = 1nF		2		ns
Minimum Input Pulse Width that Changes the Output	t_{PW}			15		ns
THERMAL CHARACTERISTICS						
Thermal-Shutdown Temperature		Temperature rising		+160		°C
Thermal-Shutdown Temperature Hysteresis				15		°C

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 3: Design guaranteed by bench characterization. Limits are not production tested.

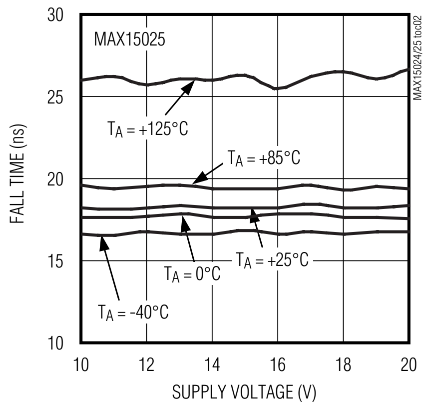
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

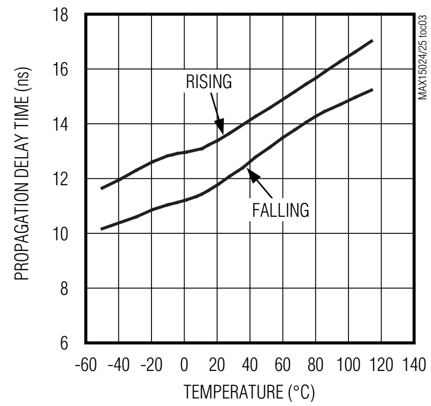
RISE TIME vs. SUPPLY VOLTAGE (DUAL DRIVER WITH 5nF LOAD)



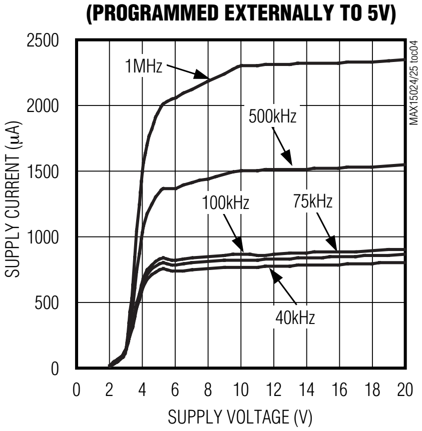
FALL TIME vs. SUPPLY VOLTAGE (WITH 5nF LOAD)



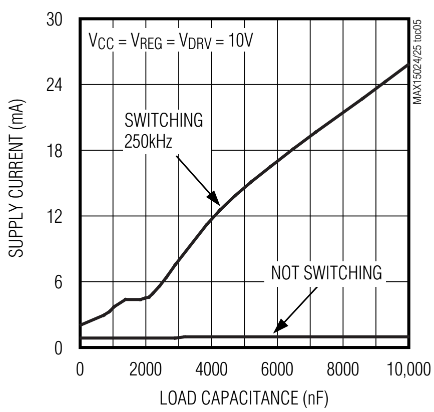
PROPAGATION DELAY TIME vs. TEMPERATURE (1nF LOAD)



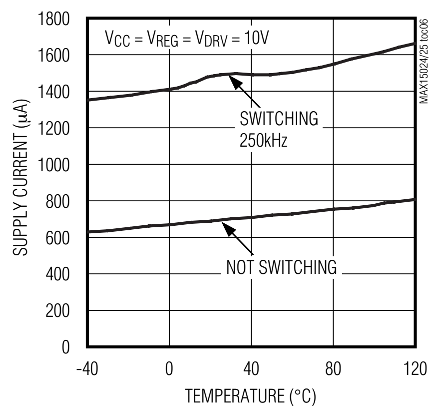
SUPPLY CURRENT vs. SUPPLY VOLTAGE (PROGRAMMED EXTERNALLY TO 5V)



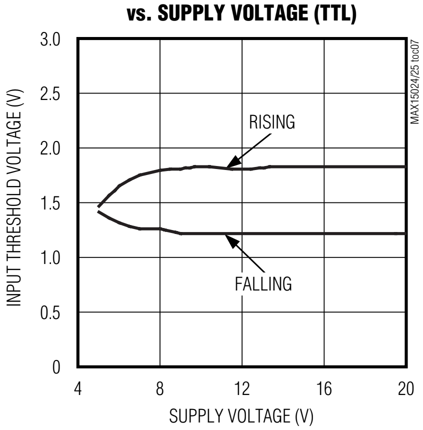
SUPPLY CURRENT vs. LOAD CAPACITANCE



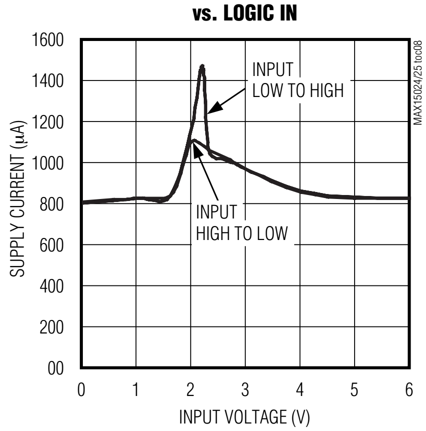
SUPPLY CURRENT vs. TEMPERATURE



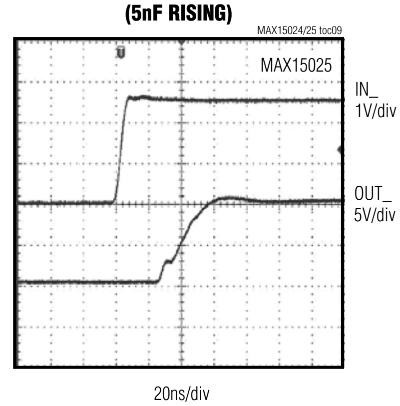
INPUT THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE (TTL)



SUPPLY CURRENT vs. LOGIC IN



LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (5nF RISING)

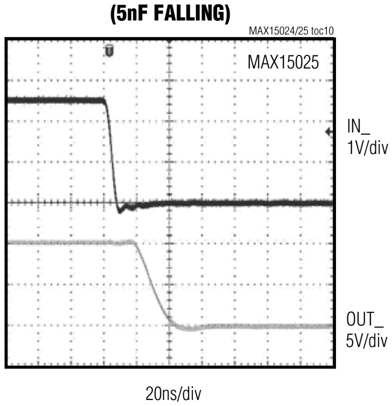


Single/Dual, 16ns, High Sink/Source Current Gate Drivers

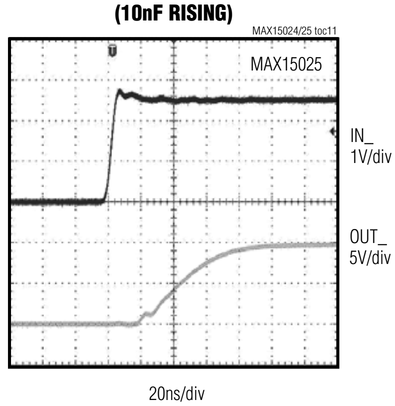
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

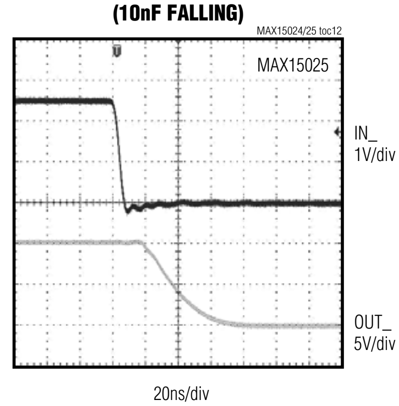
LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (5nF FALLING)



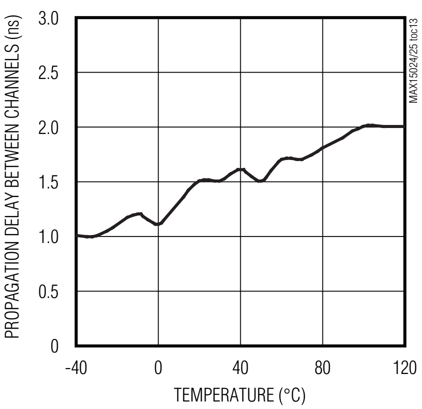
LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (10nF RISING)



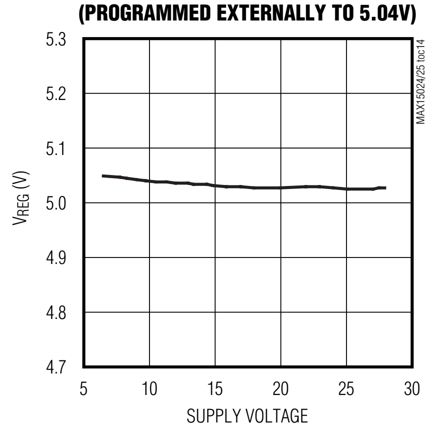
LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (10nF FALLING)



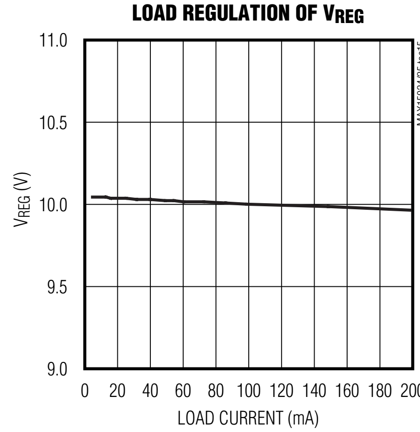
PROPAGATION DELAY MISMATCH vs. TEMPERATURE



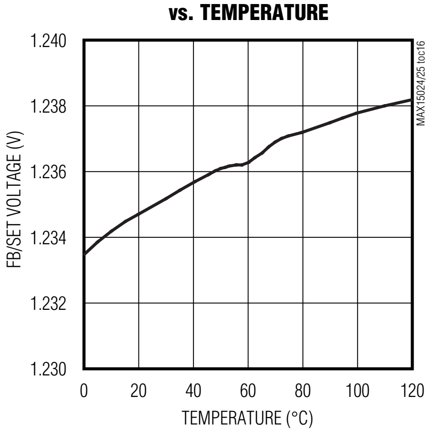
LINE REGULATION OF V_{REG} (PROGRAMMED EXTERNALLY TO 5.04V)



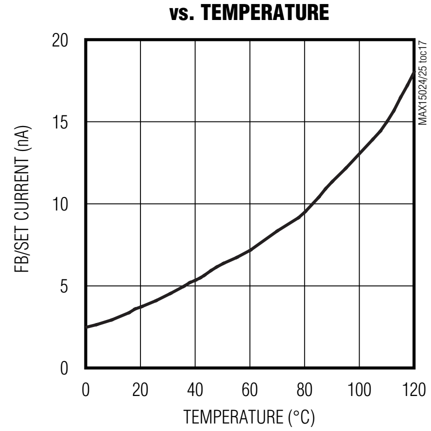
LOAD REGULATION OF V_{REG}



FB/SET VOLTAGE vs. TEMPERATURE



FB/SET CURRENT vs. TEMPERATURE



Pin Description

PIN			NAME	FUNCTION
MAX15024	MAX15025A MAX15025B MAX15025E MAX15025F	MAX15025C MAX15025D MAX15025G MAX15025H		
1	1	1	FB/SET	LDO Regulator Output Set. Feedback for V_{REG} adjustment (V_{FB} > 200mV). Connect FB/SET to GND for a fixed 10V output REG. Connect FB/SET to a resistor ladder to set V_{REG}.
2	2	2	V_{CC}	Power-Supply Input. Bypass to GND with a low-ESR ceramic capacitor of 1µF. Input of the internal housekeeping regulator and of the main REG regulator.
3	3	3	GND	Signal Ground
4	—	—	IN+	Driver Noninverting Logic Input. Connect to V_{CC} when not used.
—	4	4	IN1	Driver 1 Noninverting Logic Input
5	—	—	IN-	Driver Inverting Logic Input. Connect to GND when not used.
—	5	—	IN2	Driver 2 Noninverting Logic Input
—	—	5	$\overline{IN2}$	Driver 2 Inverting Logic Input
6	6	6	PGND	Power Ground. Sink current return. Source of the internal pulldown n-channel transistor.
7	—	—	N_OUT	Sink Output. Open-drain n-channel output. N_OUT sinks current for power MOSFET turn-off.
—	7	7	OUT2	Driver 2 Output
8	—	—	P_OUT	Source Output. Pullup p-channel output (open drain). Sources current for power MOSFET turn-on.
—	8	8	OUT1	Driver 1 Output
9	9	9	DRV	Output Driver Supply Voltage. Decouple DRV with a low ESR > 0.1µF ceramic capacitor to PGND placed in close proximity to the device. DRV can be powered independently from REG. Connect DRV, REG, and V_{CC} together when there is no need for special DRV supply sequencing and the power-MOSFET gate voltage does not need to be regulated or limited.
10	10	10	REG	Voltage Regulator Output. Connect to DRV for driving the power MOSFET with regulated V_{GS} amplitude. Bypass with a low-ESR 1µF (minimum) ceramic capacitor to GND placed in close proximity to the device to ensure regulator stability.
—	—	—	EP	Exposed Pad. Internally connected to GND. Connect to GND plane or thermal pad and use multiple vias to a solid copper area on the bottom of the PCB.

Detailed Description

The MAX15024 single gate driver's internal source and sink transistor outputs are brought out of the IC to independent outputs allowing control of the external MOSFET's rise and fall time. The MAX15024 single gate driver is capable of sinking an 8A peak current and sourcing a 4A peak current. The MAX15025 dual gate drivers are capable of sinking a 4A peak current and sourcing a 2A peak current.

An integrated adjustable low-dropout linear voltage regulator (LDO) provides gate drive amplitude control and optimization. The single gate-driver propagation delay time is minimized and matched between the inverting and noninverting inputs. The dual gate-driver propagation delay is matched between channels.

The MAX15024 has a dual input (IN+ and IN-), allows the use of an inverting or noninverting input, and is offered in TTL or CMOS-logic standards. The MAX15025 is offered with configurations of inverting and noninverting inputs with TTL or CMOS standards (see the *Selector Guide*).

The MAX15024A/B and MAX15025A/B/C/D can be powered using V_{CC} only, whereas the MAX15024C/D and MAX15025E/F/G/H can be used in two configurations:

- V_{CC} powered only
- V_{CC}, REG, and DRV are connected together

LDO Voltage Regulator Feedback Control

The MAX15024/MAX15025 include an internal LDO designed to deliver a stable reference voltage for use as a supply voltage for the internal MOSFET gate drivers. Connect the LDO feedback FB/SET to GND to set V_{REG} to a stable 10V. Connect FB/SET to a resistor-divider between V_{REG} and GND to set V_{REG}:

$$V_{REG} = V_{FB/SET} \times (1 + R2 / R1) \text{ (see Figure 2)}$$

V_{CC} Undervoltage Lockout

When V_{CC} is below the UVLO threshold, the internal n-channel transistor is ON and the internal p-channel transistor is OFF, holding the output at GND independent of the state of the inputs so that the external MOSFETs remain OFF in the UVLO condition. The UVLO threshold is 3.5V (typ) with 200mV (typ) hysteresis to avoid chattering.

When the device is operated at very low temperatures and below the UVLO threshold, the driver output could go high impedance. In this case, it is recommended adding a 10kΩ resistor to PGND to discharge the gate of the external MOSFET (see Figures 4 and 5).

Input Control

The MAX15024 features inverting and noninverting input terminals. These inputs provide for flexibility of design and use. Connect IN+ to V_{CC} when using IN- as an inverting input. Connect IN- to GND when using IN+ as a noninverting input.

Shoot-Through Protection

The MAX15024/MAX15025 provide protection that avoids any cross-conduction between the internal p-channel and n-channel devices. It also eliminates shoot-through, thus reducing the quiescent supply current.

Exposed Pad (EP)

The MAX15024/MAX15025 include an exposed pad allowing greater heat dissipation from the internal die to the outside environment. Solder the exposed pad carefully to GND or thermal pad to enhance the thermal performance.

Applications Information

Supply Bypassing, Device Grounding, and Placement

Ample supply bypassing and device grounding are extremely important because when large external capacitive loads are driven, the peak current at the V_{DRV} pin can approach 4A, while at the PGND pin, the peak current can approach 8A. V_{DRV} drops and ground shifts are forms of negative feedback for inverters and, if excessive, can cause multiple switching when the inverting input is used and the input slew rate is low. The device driving the input should be referenced to the MAX15024/MAX15025 GND. Ground shifts due to insufficient device grounding can disturb other circuits sharing the same AC ground return path. Any series inductance in the V_{DRV}, OUT_, and/or PGND paths can cause oscillations due to the very high di/dt that results when the MAX15024/MAX15025 are switched with any capacitive load. A 0.1µF or larger value ceramic capacitor is recommended for bypassing V_{DRV} to GND and should be placed as close to the pins as possible. When driving very large loads (> 10nF) at minimum rise time, 10µF or more of parallel storage capacitance is recommended. A ground plane is highly recommended to minimize ground return resistance and series inductance. Care should be taken to place the MAX15024/MAX15025 as close as possible to the external MOSFET being driven to further minimize board inductance and AC path resistance.

Power Dissipation

Power dissipation of the MAX15024/MAX15025 consists of three components: the quiescent current, capacitive charge and discharge of internal nodes, and the output current (either capacitive or resistive load). The sum of these components must be kept below the maximum power-dissipation limit. The quiescent current is 700µA typ. The current required to charge and discharge the internal nodes is frequency dependent (see the *Typical Operating Characteristics*). The MAX15024/MAX15025 power dissipation when driving a ground-referenced resistive load is:

$$P = D \times R_{ON(MAX)} \times I_{LOAD}^2$$

where D is the fraction of the period the MAX15024/MAX15025s' output pulls high, $R_{ON(MAX)}$ is the maximum on-resistance of the device with the output high (p-channel), and I_{LOAD} is the output load current of the MAX15024/MAX15025. For capacitive loads, the power dissipation for each driver is:

$$P = C_{LOAD} \times V_{DRV}^2 \times FREQ$$

where C_{LOAD} is the capacitive load, V_{DRV} is the driver supply voltage, and FREQ is the switching frequency.

Layout Information

The MAX15024/MAX15025 MOSFET drivers source and sink large currents to create very fast rise and fall edges at the gate of the switching MOSFET. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following printed-circuit board (PCB) layout guidelines are recommended when designing with the MAX15024/MAX15025:

- Place one or more 1µF decoupling ceramic capacitor(s) from V_{DRV} to PGND as close to the device as possible. At least one storage capacitor of 10µF (min) should be located on the PCB with a low resistance path to the V_{CC} pin of the MAX15024/MAX15025.
- There are two AC current loops formed between the device and the gate of the MOSFET being driven. The MOSFET looks like a large capacitance from gate to source when the gate is being pulled low. The active current loop is from MOSFET gate to OUT_ of the MAX15024/MAX15025 to PGND of the MAX15024/MAX15025, and to the source of the MOSFET. When the gate of the MOSFET is being pulled high, the active current loop is from the V_{DD} terminal of the V_{DRV} terminal of decoupling capacitor, to the V_{DRV} of the MAX15024/MAX15025, to the OUT_ of the MAX15024/MAX15025, to the MOSFET gate, to the MOSFET source, and to the negative terminal of the decoupling capacitor. Both charging current loop and discharging current loop are important. It is important to minimize the physical distance and the impedance in these AC current paths.
- Keep the device as close as possible to the MOSFET.
- In the multilayer PCB, the inner layers should consist of a GND plane containing the discharging and charging current loops.

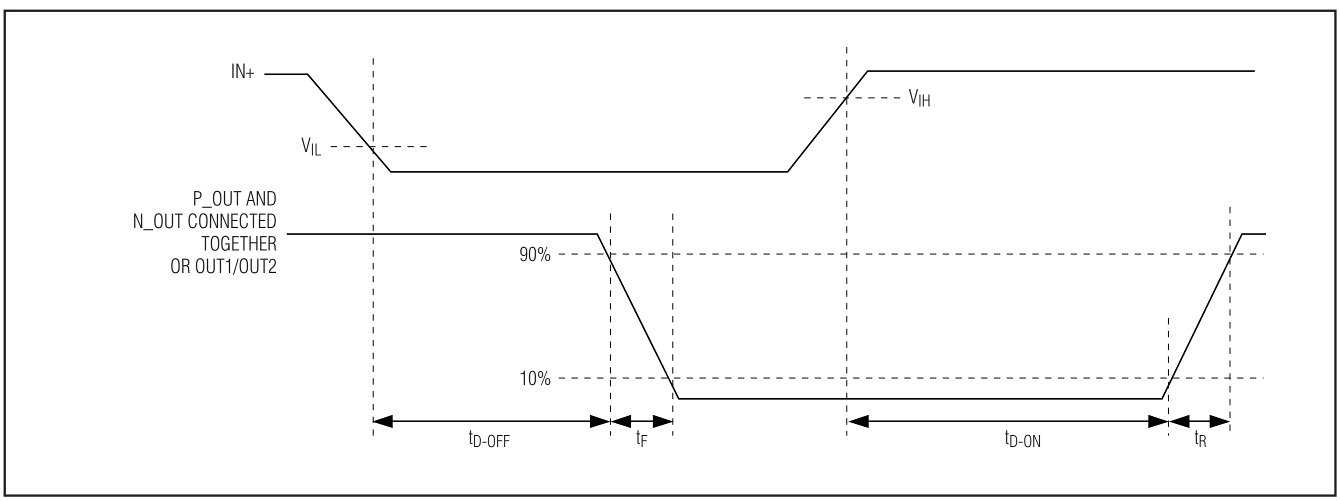


Figure 1. Timing Diagram

Single/Dual, 16ns, High Sink/Source Current Gate Drivers

Typical Operating Circuits

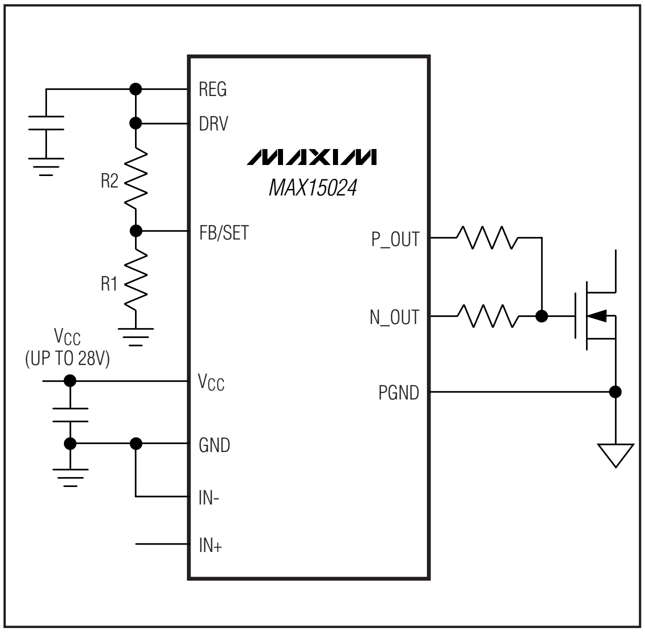


Figure 2. Connect FB/SET to GND for V_{REG} = 10V (Connect EP to GND)

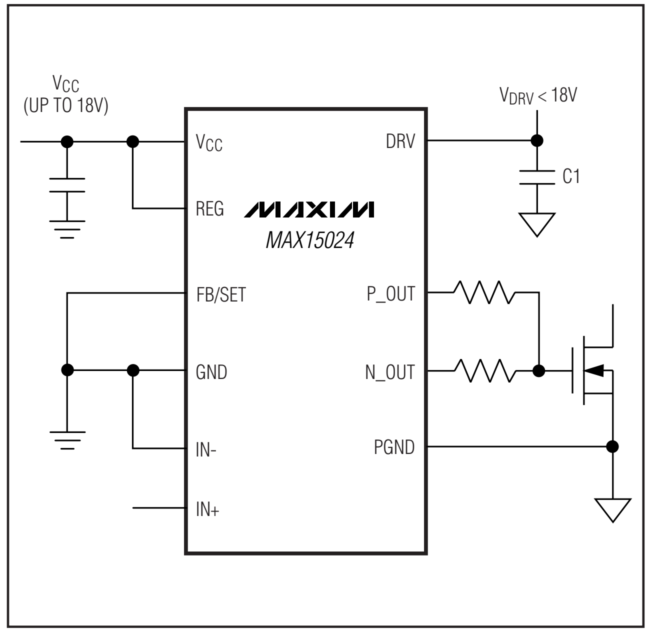


Figure 3. Operation Using a Different Supply Rail for DRV (Connect EP to GND)

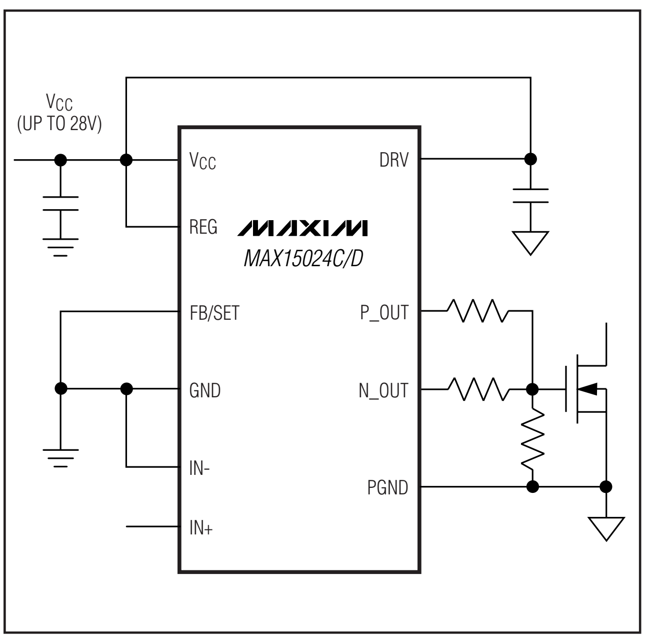


Figure 4. Operation Using a V_{CC} = DRV = REG (Connect EP to GND)

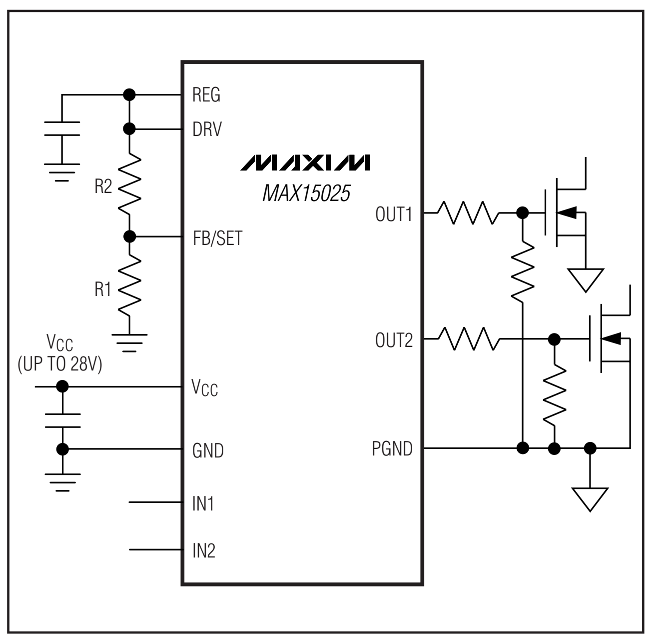
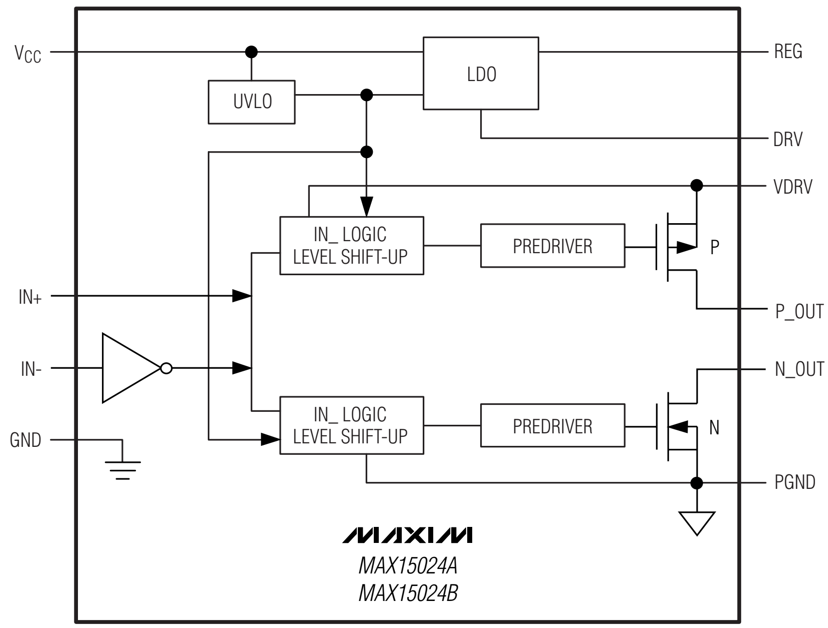
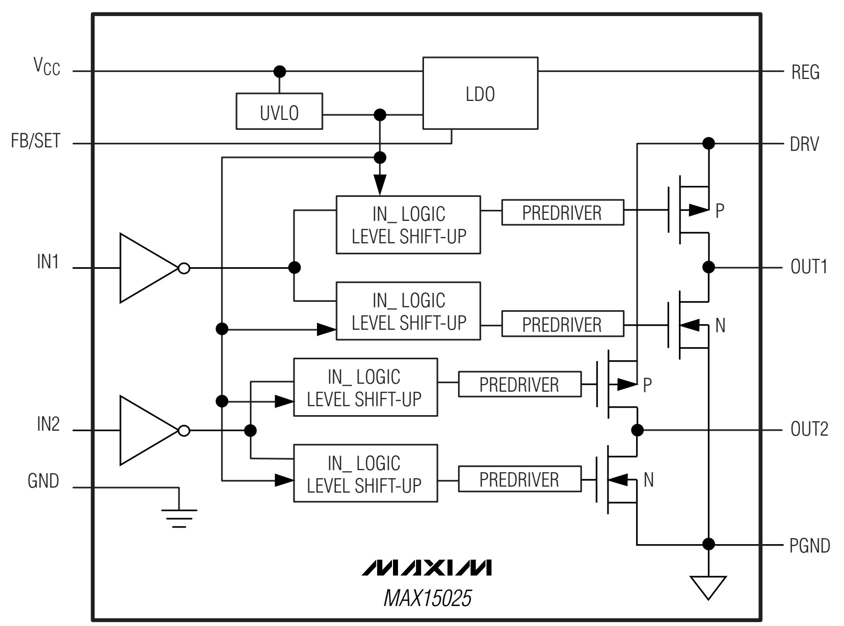


Figure 5. Connect FB/SET to GND for V_{REG} = 10V (Connect EP to GND)

Block Diagrams





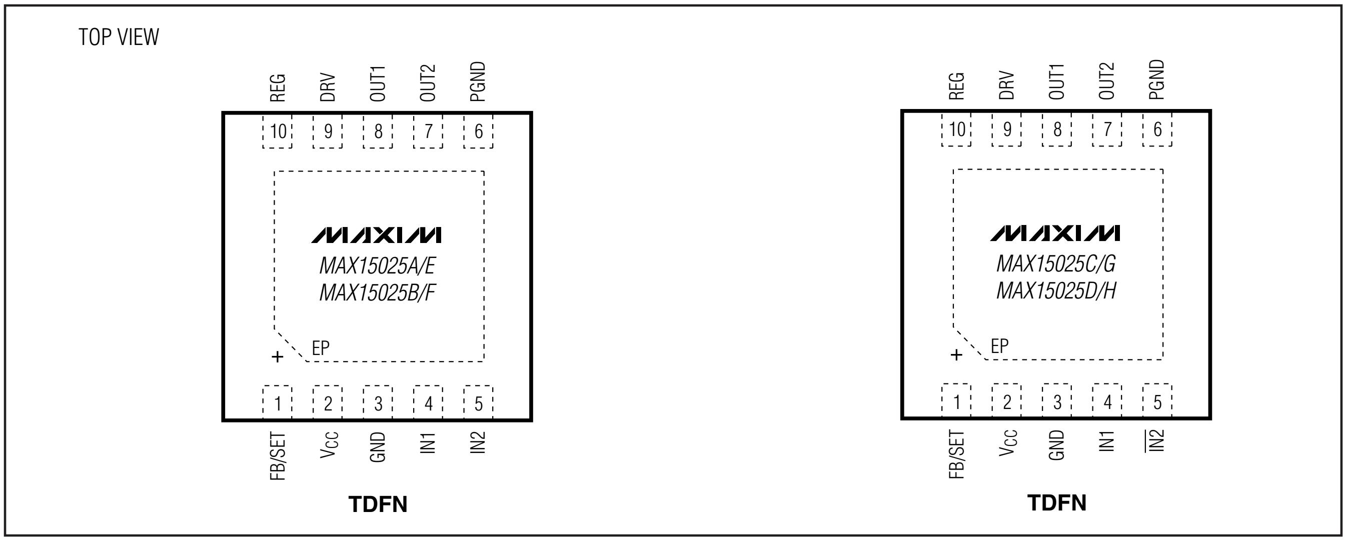
Single/Dual, 16ns, High Sink/Source Current Gate Drivers

Selector Guide

PART	NO. OF CHANNELS	PEAK CURRENTS (SINK/SOURCE)	INPUTS	LOGIC LEVELS	TOP MARK	V_{CC}-POWERED ONLY	$V_{CC} = V_{REG} = V_{DRV}$
MAX15024AATB+	1	8A/4A	Complementary	TTL	ATX	✔	—
MAX15024BATB+	1	8A/4A	Complementary	CMOS	ATY	✔	—
MAX15024CATB+	1	8A/4A	Complementary	TTL	—	✔	✔
MAX15024DATB+	1	8A/4A	Complementary	CMOS	—	✔	✔
MAX15025AATB+	2	4A/2A	Noninverting	TTL	ATZ	✔	—
MAX15025BATB+	2	4A/2A	Noninverting	CMOS	AUA	✔	—
MAX15025CATB+	2	4A/2A	Noninverting (1)/ Inverting (2)	TTL	AUB	✔	—
MAX15025DATB+	2	4A/2A	Noninverting (1)/ Inverting (2)	CMOS	AUC	✔	—
MAX15025EATB+	2	4A/2A	Noninverting	TTL	—	✔	✔
MAX15025FATB+	2	4A/2A	Noninverting	CMOS	—	✔	✔
MAX15025GATB+	2	4A/2A	Noninverting (1)/ Inverting (2)	TTL	—	✔	✔
MAX15025HATB+	2	4A/2A	Noninverting (1)/ Inverting (2)	CMOS	—	✔	✔

Note: *All devices operate in a -40°C to +125°C temperature range and come in a 10-pin TDFN package.*

Pin Configurations (continued)



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 TDFN	T1033-1	21-0137

Single/Dual, 16ns, High Sink/Source Current Gate Drivers

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/07	Initial release	—
1	3/08	Updated *Ordering Information* and *Electrical Characteristics* tables and revised *Block Diagram*.	1–6, 9, 13